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MEARS TECHNOLOGIES LAUNCHED TO RESOLVE CRITICAL ISSUE FACING THE SEMICONDUCTOR INDUSTRY

Company's Breakthrough Technology Significantly Reduces Gate Leakage for Deep Sub-Micron Processes; Aims to Extend Life of Conventional Semiconductor Manufacturing

Waltham, Mass., December 11, 2006 — For decades, the semiconductor industry has maintained a strategy of delivering chips that have doubled in performance every two years through the ongoing migration to smaller process geometries. The reduced circuit dimensions yield higher performance while requiring less power, which is critical for mobile electronics devices, a market segment fueling much of the growth in the semiconductor industry. However, the inverse power-to-performance ratio is becoming harder to sustain as circuit designs move to 65 nanometer (nm) and beyond. One factor is that the physical properties of the silicon itself are presenting a major performance limitation. As such, a new company, MEARS Technologies, has been launched to re-engineer the physical properties of silicon in order to reduce gate leakage by as much as 60 percent in NMOS transistors and up to 80 percent in PMOS transistors, while maintaining drive current for a variety of deep sub-micron processes. Through this unique approach, MEARS Technologies intends to enable semiconductor companies to continue with their aggressive device roadmaps while still leveraging the semiconductor industry's existing manufacturing infrastructure.

“Silicon devices make up approximately 95 percent of the \$250 billion semiconductor market. However, it is becoming increasingly clear that the limitations of bulk silicon are beginning to compromise the ability of CMOS manufacturing to deliver exponentially better performance at ever lower cost and power,” said Bill McClean, president of IC Insights, a leading market analyst firm tracking the semiconductor industry. “While recently introduced options offer a viable

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short-term boost in performance, the industry as a whole has been searching for a breakthrough that extends the life of CMOS and lowers power dissipation – without requiring sweeping changes in materials or huge investments in new manufacturing equipment and facilities.”

MST™ Platform Mitigates Gate Leakage

MEARS Technologies is tackling the issues of chip performance and power consumption head-on with its new MST™ Platform. Static power dissipation, also called gate leakage, can account for as much as 70 percent of the total power budget of devices manufactured at the 65 nm process node. Using a band engineering approach, MEARS Technologies has developed its patented MST Platform to dramatically reduce gate leakage, providing a tremendous advantage for all applications that benefit from reduced power consumption. In addition, the new technology will enhance drive current, which relates directly to increased semiconductor speed.

“The explosive growth of cell phones and other personal electronics devices has created conflicting demands for semiconductors with increased performance and reduced power consumption,” said Robert J. Mears, founder and president of MEARS Technologies. “The ability of the industry to respond to these demands continues to depend on the electrical properties of a single material – silicon. As chipmakers attempt to squeeze more performance out of their transistors, the fundamental properties of silicon and its native oxide have become the limiting factor. And while some approaches have been successful in addressing performance requirements, power issues continue to exist. Through a new approach to silicon engineering, we are able to alter the properties of the silicon to improve the power efficiency and speed of transistors manufactured using deep sub-micron process nodes such as 65 nm, 45 nm and beyond, while maintaining compatibility with standard CMOS manufacturing equipment that is used for the vast majority of today’s semiconductors.”

Compatible with Today’s Standard Manufacturing Processes

MEARS Technologies’ MST Platform is designed to be fully compatible with semiconductor manufacturers’ baseline processes, whether it be bulk CMOS, strained silicon or silicon-on-insulator. The power improvements are achieved through a band engineering approach that is based on a deep understanding of the quantum mechanics of modern deep-submicron devices. In

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its first implementation, MST Generation 1 is a channel replacement technology incorporating a silicon laminate, or “superlattice” layer, which requires no new materials be used in the fabrication process. This “silicon-on-silicon” solution adds only a few steps to the standard CMOS manufacturing flow — and at virtually no additional cost or impact to production yields.

About MEARS Technologies’ Management Team

MEARS Technologies’ management team combines a unique blend of materials engineering and physics expertise with a strong knowledge of semiconductor process technologies. Dr. Robert J. Mears, MEARS Technologies’ founder and president, has more than 20 years of research experience in electronics and photonics and is the inventor of the erbium-doped fiber amplifier (EDFA), which helped enable the broadband Internet. Dr. Mears leads a team that includes Scott Kreps, vice president of engineering, who has more than 20 years of experience in semiconductor product development and manufacturing with companies such as Harris Semiconductor (now Intersil) and Applied Micro Circuits Corporation (AMCC). In addition, Dr. Marek Hytha, chief scientist, has more than 15 years of experience in condensed matter physics and is the successful developer of numerous ab initio quantum mechanical techniques for the calculation of chemical and solid state properties in materials.

MEARS Technologies’ strategy is to form long-term partnerships with world-class semiconductor suppliers and manufacturers to address the issues of chip performance and power consumption at 65 nm and beyond. For more information on MEARS Technologies and the MST Platform, please call 617/219-0600 or visit www.mearstechnologies.com.

About MEARS Technologies

MEARS Technologies is an emerging materials technology company that provides advanced silicon processes and engineering services to semiconductor device manufacturers and contract foundries. The company combines a core competency in materials engineering and quantum mechanics with practical semiconductor process technology know-how to optimize the power efficiency and performance of integrated circuits manufactured on deep sub-micron processes. With a licensing model and strong patent position covering breakthrough silicon structures,

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methods and processes, MEARS Technologies enhances the fundamental electronic properties of silicon without requiring new manufacturing equipment or the use of exotic materials.

MST is a trademark of MEARS Technologies.